A Harmonic Suppression Scheme for Full Speed Range of a Two Level Inverter Fed Induction Motor Drive using Switched Capacitive Filter

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Abstract—This paper proposes a novel harmonic suppression scheme for 2-level inverter fed 3-terminal induction motor drives using switched capacitive filter. Capacitor fed H-bridges used as filters are cascaded to conventional 2-level inverter to eliminate 5th and 7th order harmonics for the full modulation range including six-step operation. For the first time 2-level dodecagonal voltage space vector is implemented with single DC supply for 3-terminal induction motor drive. Enabling the switched capacitive filtering at low voltage domain and shifting the high frequency switching to the switched capacitive filter is shown. An uniform PWM technique is shown which charges and maintains the capacitor voltages while eliminating the 5th and 7th order harmonics for the full speed range.

Index Terms—Induction motors, AC drives, pulse width modulation, DC-link, harmonics, dodecagonal, space vector.

I. INTRODUCTION

FOR low voltage medium power drives application, conventional three phase 2-level inverter fed 3-terminal induction motor drive is widely used. For operation in the full speed range of the induction motor, the inverter has to operate in the overmodulation region and the six-step mode. In overmodulation region and six-step mode operation, substantial 5th and 7th order harmonics are generated in the phase voltage. The resulting 5th and 7th harmonic phase current, produce 6th harmonic torque ripple in the motor, which deteriorates precise speed control of the machine and sometimes even lead to mechanical breakaway [1].

To suppress the 5th and 7th order harmonics from the phase voltage of the 2-level inverter, LC line filters are used. But, LC line filters adds to the size, weight and cost of the drive system. Hence, for applications like electric vehicle drives, use of LC filters to enable the machine to operate in full speed range without the effect of 5th and 7th order harmonics, is not a viable option. Additionally inverter switching frequency is also increased to suppress the harmonics, which leads to increased

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switching loss, making the drive less efficient. Different modulation techniques are also used in the overmodulation region to filter the 5th and 7th order harmonics [2], [3].

Notches are introduced in the pole voltage waveform at pre-computed angles to selectively eliminate a particular harmonic from the phase voltage [4]–[9]. Selective Harmonic Elimination (SHE) requires intensive offline as well as online computation, which in many applications is a limitation to be implemented. Moreover, notches introduced in SHE doesn't allow the six-step operation of the 2-level inverter, limiting the speed range of the drive.

Inverters switching dodecagonal (12-sided polygon) voltage space vectors has been shown to completely eliminate the 5th and 7th order harmonics from the phase voltage even for extreme 12-step operation [10]. The works in [10]–[16], have proposed several schemes for realization of multilevel dodecagonal voltage space vectors for high voltage, high power induction motor drives. However, multiple DC-supplies are used in those topologies which add up to the size of the inverter for voltage generation at specific ratios. The work in [17], shows a condition when additional DC-supplies can be replaced by capacitors for implementation of dodecagonal voltage space vectors for open-end winding configuration of IM drives. Hence, use of multiple DC-supplies are avoided in [17] for open-end winding induction motor drives.

The work presented in this paper gives a solution to overcome the mentioned problems associated with low voltage medium power 3-terminal induction motor (without requirement for open-end winding) drives, through the following contributions.

- A switched capacitive filtering scheme is proposed for the first time which eliminates 5th and 7th order harmonics from the phase voltage for the full modulation range including the overmodulation region and six-step operation of a 2-level inverter fed 3-terminal induction motor drive. Hence, the induction motor can be operated for the full speed range with complete elimination of 6th harmonic torque ripple.
- The high frequency switching is shifted to the low voltage switched capacitive filter. Thus, harmonic suppression is achieved without increase in the switching frequency of the 2-level inverter. This results in reduced switching loss with enhanced harmonic suppression, compared to 2-level inverter. The switched capacitive filter is realized

by capacitor fed H-bridges. As the capacitive filter is in low voltage domain (14.45% of DC-supply), the H-bridge switches can be implemented with low voltage devices like MOSFETS. Hence, the overall size, weight and cost of the drive can be drastically reduced when compared to the use of LC filters.

- For the first time a 2-level dodecagonal voltage space vector is implemented using single DC supply for a 3-terminal induction motor. Hence, multiple power supplies are avoided making the drive more compact for low voltage medium power applications. This also results an increase in linear modulation range by 7.79% as compared to a conventional 2-level inverter.

- An uniform modulation technique is proposed for the entire speed range of the motor while 5th and 7th order harmonics are totally eliminated. The proposed PWM technique charges the capacitors at the set voltage at startup thus avoiding any precharging circuitry. The PWM technique is also shown to maintain the capacitor voltage while 5th and 7th order harmonic is completely eliminated.

- The instantaneous phase voltage never exceeds $(2/3)V_{DC}$ for which the machine windings are rated.

II. CONDITION FOR REPLACING DC-SUPPLY WITH CAPACITOR

The work in [10], realizes dodecagonal voltage space vectors for open-end winding configuration of IM drives, using two 2-level inverters from both sides of the winding terminals with DC-bus voltages of V_{DC} and $0.366V_{DC}$. The work in [17], ensures that no active power is contributed from the secondary inverter feeding the open-end winding induction motor. Hence, the additional DC-supply can be replaced by a capacitor (controlled at voltage of $0.289V_{DC}$) as shown in Fig. 1. The condition for replacing additional DC-supplies with capacitors explained in this section is similar to [17], which was analysed for open-end winding induction motor drive. However the work presented in this paper is for 3-terminal induction motor drive, hence the vector switchings to maintain this condition are different from [17] and is explained in this section(Fig. 3). Also, in the current work three capacitors need to contolled, which is different from [17], where only one capacitor needs to be controlled.

Let the hexagonal voltage space vector that can be formed by inverter-1 in Fig. 1 be of radius V_{DC} and the radius of the resultant dodecagon that can be formed (by inverter-1 and inverter-2) be V_d (Fig. 2). If the fundamental voltages from both the possible voltage spaces are made equal, then active power contribution by the inverter-2 for the same load can be ensured to zero and hence, the DC-supply can be replaced by capacitor. For extreme step operation in hexagonal and dodecagonal voltage space, the fundamental phase voltages are $0.637V_{DC}$ and $0.659V_d$ respectively. By equating the two fundamental voltages, the radius of the dodecagon for which no active power is fed from inverter-2, is found in (1).

$$0.659V_d = 0.637V_{DC}$$
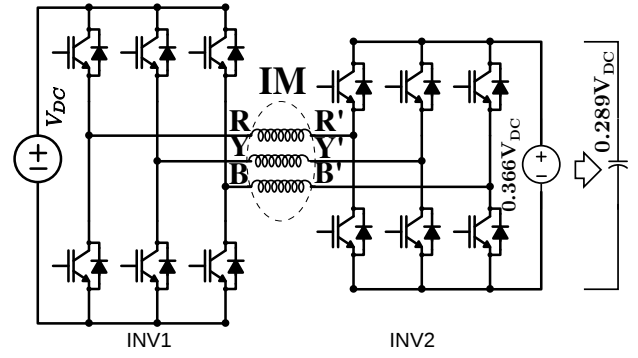
$$V_d = 0.966V_{DC} \qquad (1)$$

Fig. 1. Power circuit for dodecagonal space vector switching for open-end winding IM
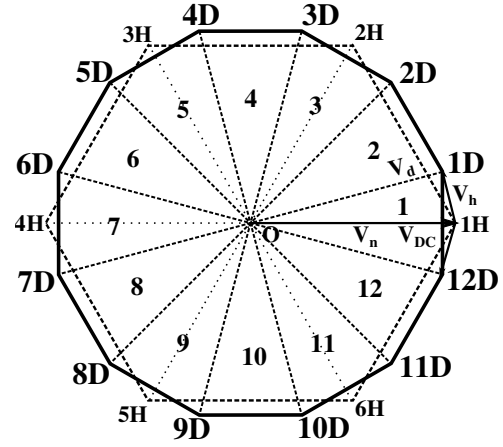

Fig. 2. Dodecagonal and hexagonal voltage space vectors which will have same fundamental voltage

Two vectors of magnitude $0.966V_{DC}$ (**1D**, **12D**), $15°$ displaced from the hexagonal voltage space vector of magnitude $\mathbf{V_{DC}}$ (**1H**) can be generated by adding vector $\mathbf{V_h}$ to the vector **1H** as shown in Fig. 3. By vectorial subtraction, the vector $\mathbf{V_h}$ is found out in (2).

$$\mathbf{V_h} = 0.966V_{DC}\angle 15° - V_{DC}\angle 0°$$

$$\mathbf{V_h} = 0.259V_{DC}\angle -75° \qquad (2)$$

The vector $\mathbf{V_h}$ is generated in time average sense, by switching between adjacent vectors $\mathbf{V_{n1}}(\mathbf{5'})$ and $\mathbf{V_{n2}}(\mathbf{4'})$ with a duty ratio of k. As the H-bridge capacitor stage forms a 3-level structure, the magnitude of $\mathbf{V_{n1}}$ and $\mathbf{V_{n2}}$ are $2V_C$(where, V_C is equal to capacitor voltage) and $1.732V_C$ respectively (Fig. 3). From the volt-second balance the value of V_C and k are found out.

$$0.259V_{DC}\angle -75°\cdot T_1 = 2V_C\angle 120°\cdot kT_1 + 1.732V_C\angle 90°\cdot (1-k)T_1 \qquad (3)$$

Resolving (3) into $\alpha - \beta$ axes and simplifying we get:

$$0.259V_{DC}\cos 105° = 2kV_C\cos 120° + (1-k)1.732V_C\cos 90° \qquad (4)$$

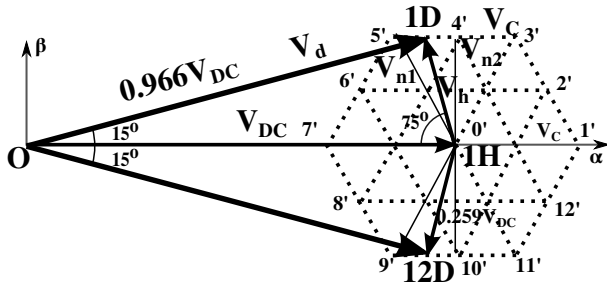$$0.259V_{DC}\sin 105° = 2kV_C\sin 120° + (1-k)1.732V_C\sin 90° \qquad (5)$$

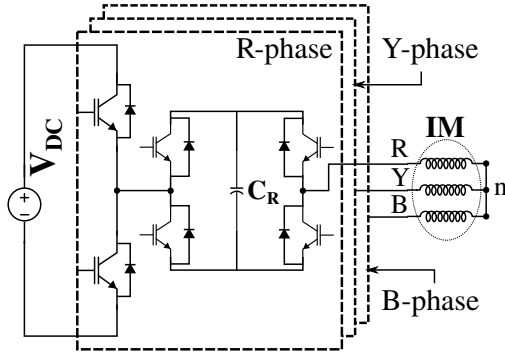Fig. 3. The vectorial construction of the dodecagonal voltage space vectors

Fig. 4. Power circuit for dodecagonal space vector switching for star connected IM

From (4) and (5) we get:

$$V_C = 0.1445V_{DC} \tag{6}$$

$$k = 0.464 \tag{7}$$

Hence, the H-bridge capacitor voltage has to be controlled at $0.1445V_{DC}$ to generate the dodecagonal vectors for 5th and 7th order harmonic elimination.

III. POWER CIRCUIT WITH SWITCHED CAPACITOR FILTER

The aim of this work is to generate the vectors as explained in previous section, for star connected IM. The open-end winding configuration enables inherent voltage vector subtraction. When these vectors are to be fed from one side of the winding, the vector subtraction will be substituted by vector addition. The voltage vector addition is possible for star connected IM, if the capacitors are connected in H-bridge configuration cascaded to 2-level configuration for each phase as shown in Fig. 4. Hence, the vectors $\mathbf{V_{n1}}$ and $\mathbf{V_{n2}}$ (Fig. 3) will be switched by the cascaded stage of capacitors connected in H-bridge configuration, to form the average vector $\mathbf{V_h}$ which will add up to the 2-level hexagonal vectors ($\mathbf{1H}, \mathbf{2H}, ..\mathbf{6H}$) to form the dodecagonal vectors $\mathbf{1D}, \mathbf{2D}, ...\mathbf{12D}$.

As the cascaded capacitor connected H-bridge stage can form a 3-level structure [18], to generate active vectors of magnitude $0.289V_{DC}$, the capacitor voltage can be equal to half that magnitude, $0.1445V_{DC}$. Hence, with this topology, an added advantage of lesser voltage stress for H-bridge switches and less dV/dt in pole voltage can be achieved. In Fig. 3, it is seen that the projection of the outer vector $\mathbf{V_{n2}}$ is always zero to the main 2-level primary vector $\mathbf{1H}$, as the vector $\mathbf{V_{n2}}$ of the 3-level configuration, lies at the mid-point of the sector
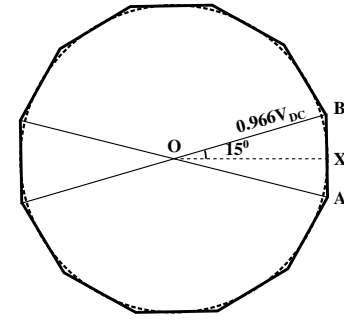

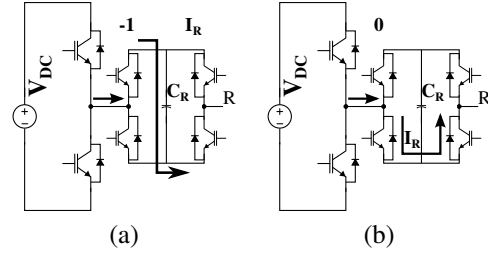Fig. 5. Circle inscribed by the maximum voltage space vector for dodecagonal voltage space

Fig. 6. H-bridge state for a particular current direction. (a) H-bridge state is -1, capacitor getting charged; (b) H-bridge state is 0, capacitor is bypassed

$3'0'5'$. Hence, the instantaneous phase voltage never exceeds $(2/3)V_{DC}$(maximum phase voltage for conventional 2-level inverter), for which the machine windings are rated.

In linear modulation range, the maximum voltage space vector that can be realized by PWM for dodecagonal voltage space vector will have a radius equal to that of the inscribed circle for the dodecagon as shown in Fig. 5. The radius of the inscribed circle $\mathbf{OX}$, is computed in (8).

$$\mathbf{OX} = \mathbf{OB} \cos 60°$$

$$OX = 0.966V_{DC} \times 0.966 = 0.933V_{DC} \tag{8}$$

From (8), the peak of the fundamental of the phase voltage is computed in (9).

$$V_{phase,pk} = (2/3)0.933V_{DC} = 0.622V_{DC} \tag{9}$$

Hence, the maximum modulation index possible is 0.622 in linear modulation range. In 2-level inverter the maximum modulation index in linear range possible is 0.577. Hence, an increase of 7.79% in maximum modulation index in linear range is obtained with the proposed topology.

IV. CAPACITOR VOLTAGE CONTROL

The cascaded layer of capacitor connected H-bridge can either add (1), subtract (-1) or bypass (0) the capacitor voltage over the 2-level pole voltage. For a given direction of the load current the H-bridge states -1 and 0 will have charging effect and no effect respectively, on the capacitor voltage as shown in Fig. 6.

To synthesize vector $\mathbf{1D}$, the capacitor connected H-bridges has to add the vector $\mathbf{V_h}$ to the 2-level vector $\mathbf{1H}$. Consider, the vector $\mathbf{1D}$ to be generated for duration T_1. Hence, the H-bridges has to apply $\mathbf{5'}$ for kT_1 and $\mathbf{4'}$ for $(1 - k)T_1$. $\mathbf{5'}$
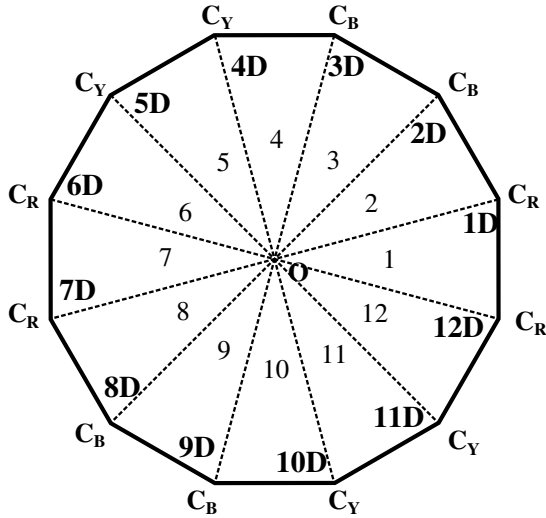
Fig. 7. Zone of control of the individual phase capacitors.

Fig. 8. Voltage controller for the capacitors.

Fig. 9. PWM scheme for the proposed inverter

is formed by the H-bridge state of (-11-1) and $\mathbf{4'}$ formed by the H-bridge states of (01-1). It can be observed that while switching $\mathbf{5'}$ and $\mathbf{4'}$, the phase current will have charging and byapassing effect respectively, on the R-phase capacitor C_R. The voltage controller modulates the value of k based on current value of C_R voltage, to control the voltage of C_R when vector $\mathbf{1D}$ is generated. Similarly, other phase capacitor voltages are controlled when other vectors of the dodecagons are generated. Depending on the sector number, the appropriate capacitors can be controlled as shown in Fig. 7. It should be noted that when vectors $\mathbf{5'}$ and $\mathbf{4'}$ are applied for generation of dodecagonal vector $\mathbf{1D}$, switching states 1 and -1 is applied continuously for C_Y and C_B respectively. Hence, capacitors C_Y and C_B will see the natural ripple due to the phase current of the machine when vector $\mathbf{1D}$ is generated. C_Y and C_B can be controlled when vectors $(\mathbf{4D}, \mathbf{5D}, \mathbf{10D}, \mathbf{11D})$ and $(\mathbf{2D}, \mathbf{3D}, \mathbf{8D}, \mathbf{9D})$ are generated respectively as shown in Fig. 7.

Three seperate integral controllers are implemented for the capacitor voltages of three phases. They give the outputs k_R, k_Y, k_B according to the respective capacitor voltage feedback. The sector number is used to multiplex the value of k to the corresponding controller outputs as shown in Fig. 8.

The worst case capacitor ripple will occur for extreme 12-step(50Hz) operation. At 50Hz(time period of 20ms) each active vector is being switched for $30°$ duration(1.67ms) Hence, the capacitor has to be sized for 1.67ms. Thus, the size of the capacitor can be determined by (10).

$$C = \frac{T_{30°} I_{rated}}{\triangle V_C} \qquad (10)$$

V. PWM GENERATION

To calculate the active vector timing duration the reference voltage vector is required. Once, reference voltage vector is obtaine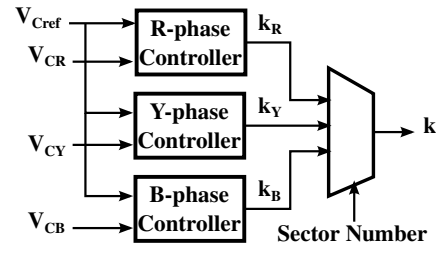d it can be resolved into V_α, V_β. The active vector timings can be calculated as shown below [13], where S is the sector number:
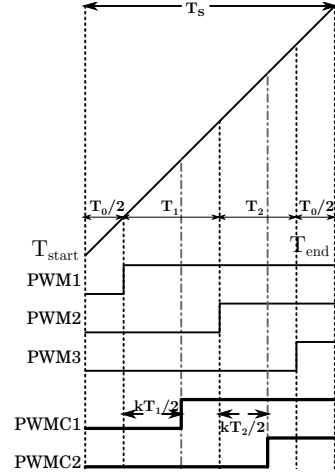
$$T_1 = \frac{2T_s}{V_d}[\sin(S \cdot 30^o - 15^o) \cdot V_\alpha - \cos(S \cdot 30^o - 15^o) \cdot V_\beta]$$

$$T_2 = \frac{2T_s}{V_d}[-\sin((S-1)\cdot 30^o - 15^o)\cdot V_\alpha - \cos(S\cdot 30^o - 15^o)\cdot V_\beta]$$

$$T_0 = T_s - T_1 - T_2 \qquad (11)$$

The active vector durations and the duty ratio k is sampled at the start of the sampling interval. Depending on sector number switching state decoders generate the switching states for the primary and secondary inverters.

Once, the active vector time durations are calculated and k is sampled at T_{start} of a sampling interval (Fig. 9), PWM1, PWM2 and PWM3 are generated, which gives the active vector duration information to the switching state decoder. PWMC1 and PWMC2 gives the information of k to the switching state decoder for the H-bridges. The PWM scheme is shown in Fig. 9. The switching state decoder, decodes the switching states from the sector number information and drives the gate driver of the switches. Based on the vector formation scheme explained in previous sections the switching table is shown in Table I. The 2-level inverter and H-bridge switching states required to generate a particular vector in the dodecagonal vector space is shown in Table I. For the 2-level inverter $\mathbf{1}$ indicates the pole voltage connected to the positive rail of the DC-supply and $\mathbf{0}$ indicates the pole voltage connected to the negative rail of the DC-supply. For the H-bridge states, $\mathbf{1}, \mathbf{-1}, \mathbf{0}$ indicate capacitor voltage addition, subtraction and

TABLE I
SWITCHING STATES FOR 2-LEVEL INVERTER AND CASCADED H-BRIDGE FOR DODECAGONAL VOLTAGE SPACE VECTOR FORMATION

ACTIVE VECTORS	2-LEVEL	H-BRIDGE	
		k	(1-k)
1D	100	-11-1	01-1
2D	110	1-11	1-10
3D	110	-111	-110
4D	010	1-1-1	10-1
5D	010	-1-11	-101
6D	011	11-1	01-1
7D	011	1-11	0-11
8D	001	-11-1	-110
9D	001	1-1-1	1-10
10D	101	-111	-101
11D	101	11-1	10-1
12D	100	-1-11	0-11

bypassing over the 2-level pole voltage respectively.

VI. RESULTS

The experiment is performed on a 3-phase 3.7kW star connected induction motor at no-load. V/f profile is maintained for speed control of the motor. The timing calculations, voltage controllers and current direction sensing are done in TMS320F2812 DSP. The sector and PWM information is communicated to the switching state decoder, which generates the driving signal for the switches. Before the switching signal is fed to the gate drivers, a dead time of $2\mu s$ is provided between the complementary switching signals. The switching state decoder and the dead time blocks are implemented in Xilinx Spartan-3 XC3S200 FPGA as shown in Fig. 10. 75A, 1200V Semikron SKM75GB12T4, IGBT based half-bridge modules are used for the 2-level inverter and 35A, 1200V FGA25N120ANTD IGBTs are used for the H-bridge switches. Considering the DC-bus to be 200V, the set value of the capacitor becomes 28.9V. The rated current for 3.7kW machine is approximately 5A and allowing a 5% ripple in the capacitor voltage, the value of the capacitor from (10) equates to $5800\mu F$. Since, we are operating only at no-load $4400\mu F$ capacitors are used for the H-bridge connected capacitors per phase. The steady state waveforms at 10Hz, 30Hz, 40Hz and extreme 12-step operation at 50Hz are shown in Fig. 11. The waveform for 10Hz is recorded with 4 samples per sector of the dodecagon or 48 samples in a fundamental cycle. The waveforms for 30Hz and 40Hz are recorded with 2 samples per sector of the dodecagon or 24 samples in a fundamental cycle. Synchronous PWM was used for all the frequency of operation. The normalized harmonic spectrum of the phase voltage is shown for 10Hz, 30Hz, 40Hz and 50Hz in Fig. 12. The harmonic analysis is done at 24 samples per fundamental cycles for 10Hz, 30Hz and 40Hz. From Fig.11d it can be seen that the primary inverter is operating at full modulation index(6-step) while the 5th and 7th order harmonic is totally eliminated from the phase voltage (as shown in Fig. 12d). The steady state voltage ripple in the H-bridge capacitors
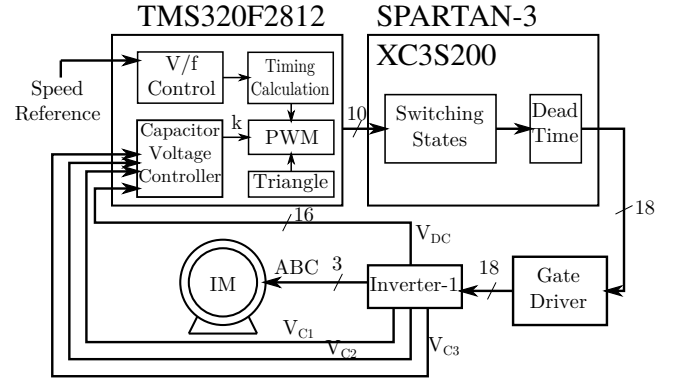

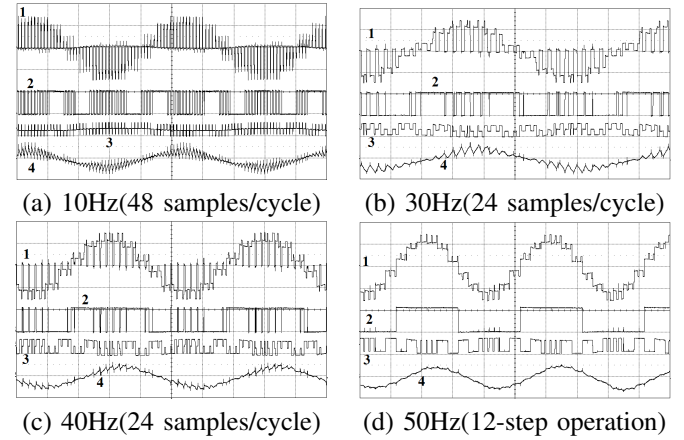Fig. 10. Block diagram of the experimental setup of the IM drive

(a) 10Hz(48 samples/cycle) (b) 30Hz(24 samples/cycle)

(c) 40Hz(24 samples/cycle) (d) 50Hz(12-step operation)

Fig. 11. Steady state experimental waveforms at no-load. (a) 1: Phase voltage(100V/div), 2: 2-level inverter pole voltage(200/div), 3: H-bridge voltage(100V/div), 4: Phase current(1A/div). Timescale-20ms/div. (b) 1: Phase voltage(100V/div), 2: 2-level inverter pole voltage(200V/div), 3: H-bridge voltage(100V/div), 4: Phase current(1A/div). Timescale-5ms/div. (c) 1: Phase voltage(100V/div), 2: 2-level inverter pole voltage(200V/div), 3: H-bridge voltage(100V/div), 4: Phase current(1A/div). Timescale-5ms/div. (d) 1: Phase voltage(100V/div), 2: 2-level inverter pole voltage(200V/div), 3: H-bridge voltage(100V/div), 4: Phase current(1A/div). Timescale-5ms/div.
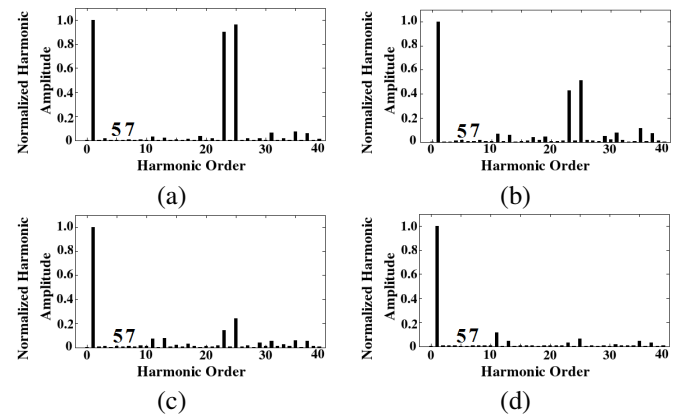

(a)

(b)

(c)

(d)

Fig. 12. Normalized harmonic spectrum for phase voltages at: (a) 10Hz, (b) 30Hz, (c) 40Hz and (d) 50Hz
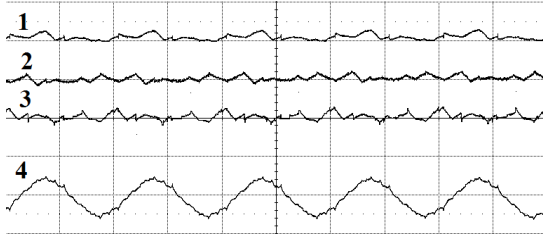
Fig. 13. Steady state H-bridge capacitor ripple at 50Hz. 1: R-phase capacitor voltage ripple(2V/div), 2: Y-phase capacitor voltage ripple(1V/div) 3: B-phase capacitor voltage ripple(1V/div), 4: Phase current(1A/div)
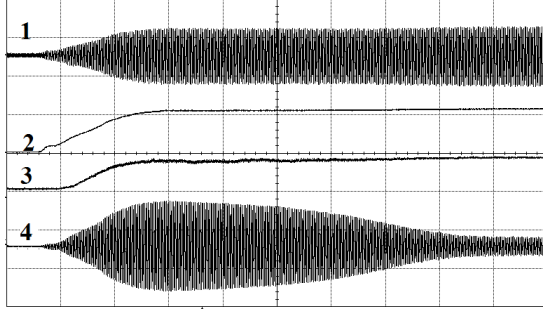

Fig. 14. Transient waveform during motor startup. 1: Phase voltage(100V/div), 2: DC-bus voltage(200V/div) 3:H-bridge capacitor voltage(30V/div), 4: Phase current(2A/div)
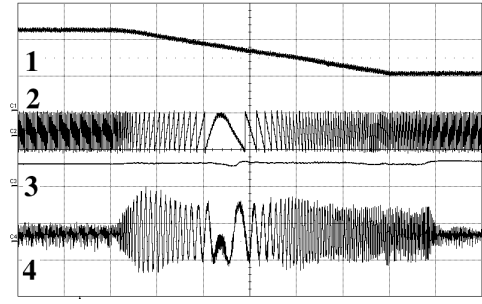

Fig. 15. Transient waveform during motor speed reversal from 48Hz to -48Hz. 1: Machine speed(2500rpm/div), 2: Rotor Position(6.28rad/div) 3:H-bridge capacitor voltage(40V/div), 4: Phase current(2A/div), Time: 1s/div
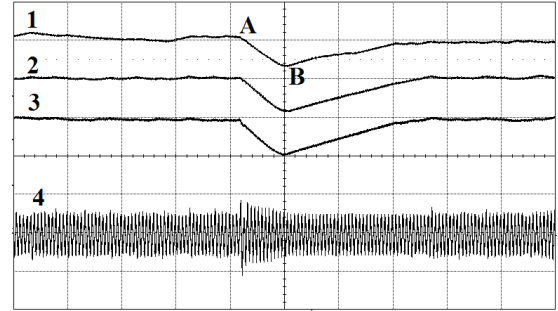

Fig. 16. Transient waveform during capacitor voltage controller reset and set operation. 1: R-phase capacitor voltage(10V/div), 2: Y-phase capacitor voltage(10V/div) 3:B-phase capacitor voltage(10V/div), 4: Phase current(2A/div)

of the individual phases are shown in Fig. 13. It can be seen that the capacitor voltage is controlled for a duration equivalent to $120°$ in the fundamental cycle, rest of the duration it is having a 6th harmonic ripple as shown in Fig. 13. From Fig. 13 it can also be observed that the voltage ripple (approximately 1V with set voltage at 28.9V) in the capacitor is approximately $0.7\%(\leq5\%)$, which is well within acceptable limits. The current THD, for extreme 12-step operation(50Hz) as shown in Fig. 13 is 14.52%. In Fig. 14 the transient voltage, current, DC-bus and capacitor voltage during motor startup is recorded. It can be seen that the voltage controller builds up the capacitor voltage to 0.1445 times the DC-bus voltage. Hence, the H-bridge capacitors need no precharging circuitry. In Fig. 15, the closed loop transient waveform for machine speed reversal is shown. The machine speed is reversed from 48Hz to -48Hz. The smooth phase reversal can be seen from the phase current and the rotor position waveform. It can be seen that even during reversal the H-bridge capacitor voltage is tightly controlled at 28.9V (14.45% of DC bus voltage of 200V).

In Fig. 16, the effectiveness of the voltage controller is shown. At A, the controller is disabled and the integrator of the integral controller is reset. It can be seen that the capacitor discharges. At B, the controller is again enabled and the capacitor voltage quickly builds up to the reference set.

In Table II the WTHD [19] comparison of phase voltages for the proposed inverter and conventional 2-level inverter is shown. The switching frequency of the 2-level inverters for both the proposed inverter and conventional case is kept constant according to the frequency of operation. It is evident that harmonic content in the phase voltage has been drastically reduced with the switched capacitor filters without the need

of higher switching frequency for the 2-level inverter. The WTHD was computed as per (12), where V_1 indicates the peak of fundamental voltage and V_h is the peak of the voltage of harmonic order h.

$$WTHD = \frac{1}{V_1}\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_h}{h}\right)^2} \qquad (12)$$

Table III compares the switching frequencies of the 2-level inverter and the capacitor fed H-bridges at various frequency of operation. It is clearly seen that the DC supply connected two-level inverter is switching at lower switching frequency and the harmonic suppression is done by the H-bridge capacitive filter, which is switching at higher frequency. The voltage level of the capacitive filter is just 14.45% of the DC supply. If comparable harmonic reduction is required for standard two-level inverter, then the inverter switching frequency has to be increased. Thus, qualitatively it can be said that the switching loss of the proposed inverter with switched capacitive filter,

TABLE II
WTHD OF PHASE VOLTAGE

| Frequency(Hz) | Phase Voltage WTHD(%) | |
	Proposed Inverter	2-level Inverter
10	1.54	2.98
20	0.86	2.40
30	0.83	1.89
40	0.82	1.70
50	1.26	3.93

TABLE III
SWITCHING FREQUENCY COMPARISON OF 2-LEVEL
INVERTER AND CAPACITOR FED H-BRIDGE FILTER

Frequency(Hz)	Samples/Cycle	Switching Frequency(Hz)	
		2-level	H-bridge
10	48	350	880
20	48	700	1760
30	24	570	1350
40	24	760	1800
50	12	50	550

is reduced compared to standard two-level inverter, while achieving substantial harmonic reduction.

VII. CONCLUSION

A novel harmonic suppression scheme is proposed in this work using switched capacitive filter for 2-level inverter fed 3-terminal induction motor drive, which is commonly used in low voltage medium power drives applications. The salient features of this work are as follows.

- 5th and 7th order harmonic elimination for the full modulation range including six-step operation of the 2-level inverter fed motor drive, using switched capacitive filter.
- An uniform PWM technique for the entire speed range which not only charges and maintains the capacitor voltage, but also eliminates the 5th and 7th order harmonics from the phase voltage.
- Shifting high frequency switching to low voltage capacitor fed H-bridges, thus reducing the switching loss while harmonics are getting suppressed.
- Implementation of single DC supply fed 2-level dodecagonal voltage space vector for 3-terminal induction motor drive for the first time. This also ensures an increase in linear modulation range by 7.79% as compared to 2-level inverter.
- Reduction in the H-bridge capacitor voltage to just 14.45% of DC supply, thus making the switched capacitor H-bridge filtering stage more compact and less expensive compared to LC filters.
- The instantaneous phase voltage never exceeds $(2/3)V_{DC}$, for which the machine windings are rated.
- In case of fault in the H-bridge filter, the H-bridges can be bypassed and the driver can be operated by the 2-level inverter.

The mentioned salient features of the proposed work makes it a compact and cost effective solution for harmonic suppression in low voltage medium power drives applications where precise speed control is critical, like electric vehicle applications.

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